



datasheet
PRELIMINARY SPECIFICATION
standalone TV encoder

OV430

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TV encoder for VGA sensors

datasheet (LQFP)
PRELIMINARY SPECIFICATION

version 1.0
may 2010

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applications

- stand alone TV encoder for VGA sensors

ordering information

- **OV00430-L48G** (lead-free)
48-pin LQFP

features

- OV430 stand alone TV encoder for VGA sensors digital video to PAL or NTSC
- sensors supported: OV7740, OV7720/OV7725, OV7675 and OV7739
- SCCB interface support
- embedded high bandwidth DAC
- external system clock or independent crystal operation
- YUV4:2:2 8-bit input digital video port (DVP)

key specifications

- **power supply:**
 - core: 1.2V \pm 10%
 - I/O: 3.3V \pm 10%
 - analog: 3.3V \pm 10%
- **temperature range:** TBD
- **power requirements:** TBD
- **package dimensions:** 7 mm x 7 mm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV430 bridge chip. The package information is shown in **section 6**.

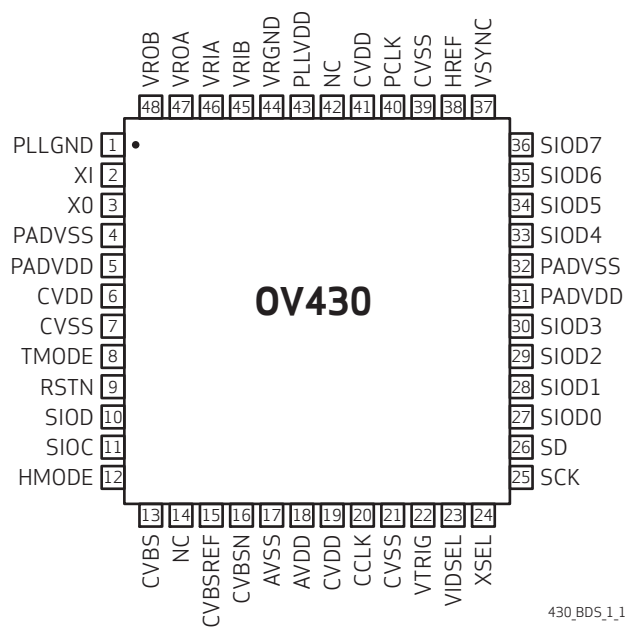
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
01	PLLGNDD	ground	PLL analog ground
02	XI	input	crystal/oscillator input
03	XO	output	crystal/oscillator output
04	PADVSS	ground	I/O ground
05	PADVDD	power	I/O power supply at 3.3V
06	CVDD	power	digital core power supply at 1.2V (coming either from the internal regulator or external source)
07	CVSS	ground	digital core ground
08	TMODE	input	test mode enable
09	RSTN	input	system reset, active low
10	SIOD	I/O	SCCB data
11	SIOC	I/O	SCCB clock
12	HMODE	input	host mode enable
13	CVBS	output	composite video positive differential
14	NC	—	no connect
15	CVBSREF	reference	reference voltage (connected to ground using 1.35K ohm resistor)
16	CVBSN	output	composite video negative differential
17	AVSS	ground	internal DAC analog ground
18	AVDD	power	internal DAC analog power supply at 3.3V
19	CVDD	power	digital core power supply at 1.2V (coming either from the internal regulator or external source)
20	CCLK	I/O	reference clock to external sensor chip
21	CVSS	ground	digital core ground
22	VTRIG	I/O	internal VSYNC output

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
23	VIDSEL	I/O	mode select 0: NTSC 1: PAL
24	XSEL	I/O	mode select 0: 24.54Mhz 1: 27Mhz
25	SCK	I/O	E2PROM clock
26	SD	I/O	E2PROM data
27	SIOD0	I/O	sensor digital video data0
28	SIOD1	I/O	sensor digital video data1
29	SIOD2	I/O	sensor digital video data2
30	SIOD3	I/O	sensor digital video data3
31	PADVDD	power	I/O power supply at 3.3V
32	PADVSS	ground	I/O ground
33	SIOD4	I/O	sensor digital video data4
34	SIOD5	I/O	sensor digital video data5
35	SIOD6	I/O	sensor digital video data6
36	SIOD7	I/O	sensor digital video data7
37	VSYNC	I/O	sensor digital video vertical SYNC
38	HREF	I/O	sensor digital video horizontal reference
39	CVSS	ground	digital core ground
40	PCLK	I/O	video pixel clock from sensor
41	CVDD	power	digital core power supply at 1.2V (coming either from the internal regulator or external source)
42	NC	–	no connect
43	PLLVD	power	PLL analog power supply at 1.2V
44	VRGND	ground	internal regulator analog ground
45	VRIB	power	internal regulator power supply at 3.3V (from I/O pad)
46	VRIA	power	internal regulator power supply at 3.3V (from I/O pad)
47	VROA	power	internal regulator power output at 1.2V (to digital core and PLL)
48	VROB	power	internal regulator power output at 1.2V (to digital core and PLL)

figure 1-1 pin diagram



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2 system level description

2.1 overview

The OV430 is a highly integrated TV encoder chip. It has on-chip video DAC that provides NTSC and PAL CVBS video signal output. The OV430 supports a VGA digital sensor input in YUV 4:2:2 data format at different frame rates. It provides a frame-rate conversion mechanism.

figure 2-1 OV430 system block diagram

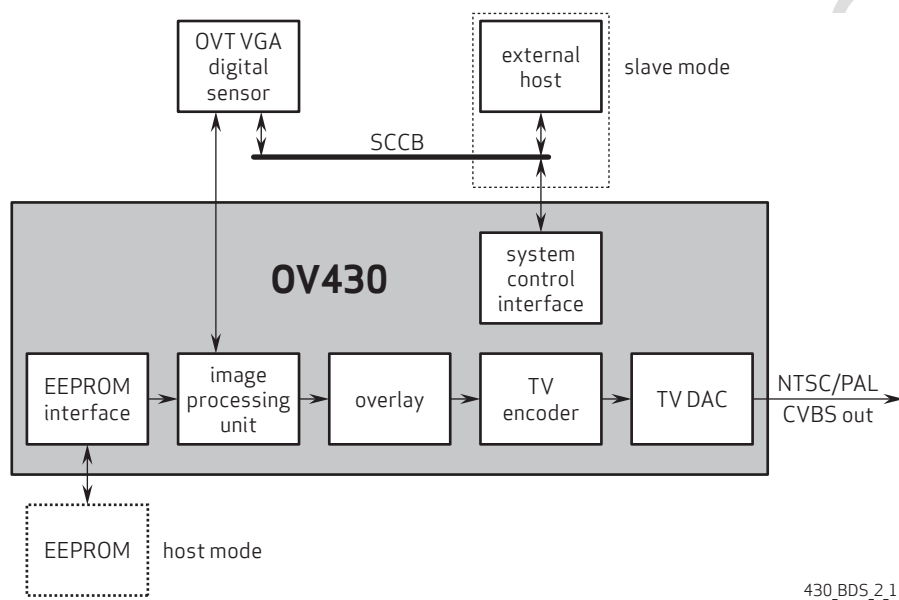
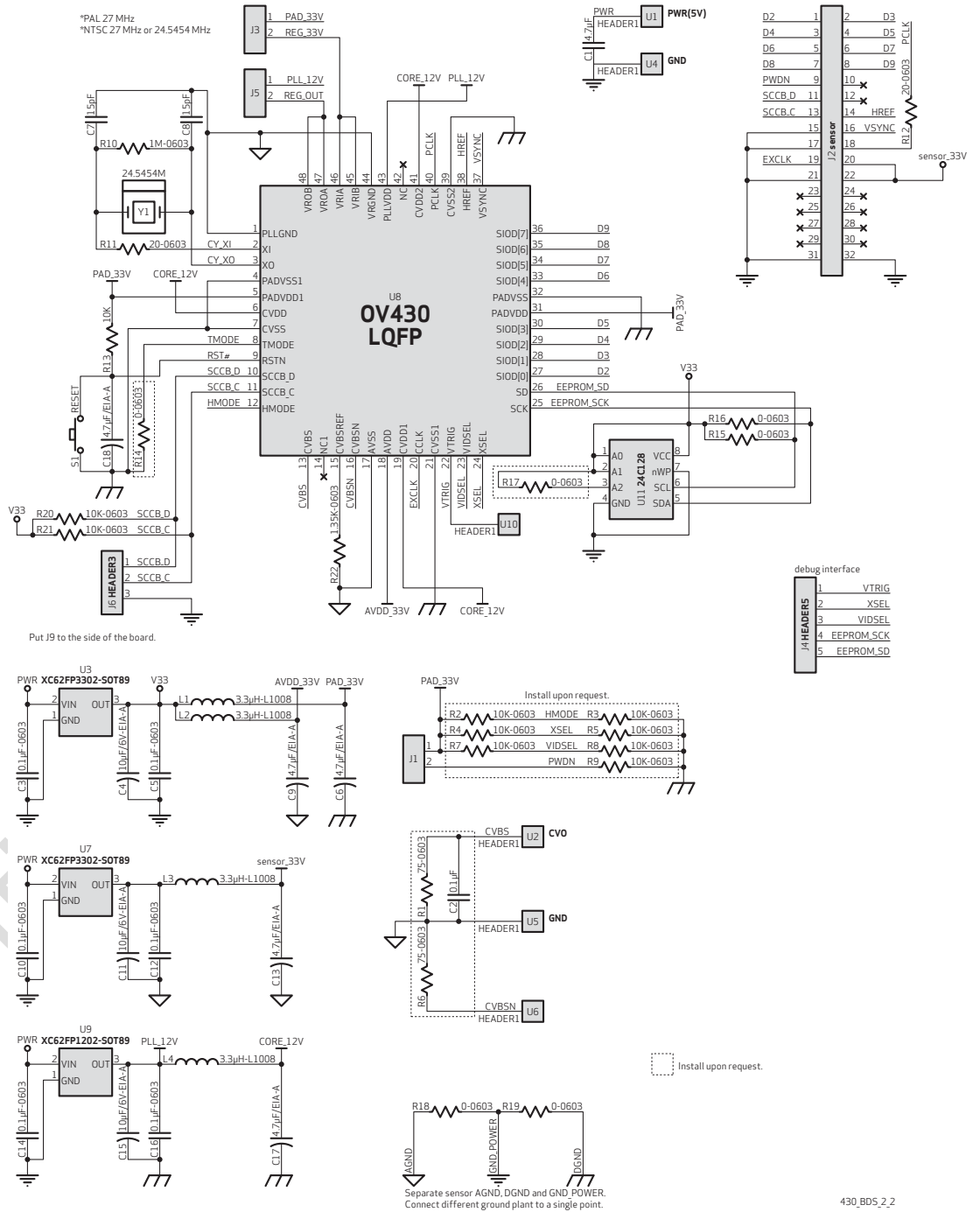


figure 2-2 OV430 reference schematic



2.2 power management

The OV430 has a free running clock. There is no power-saving or suspend mode designed in this device.

2.2.1 power supply

The OV430 takes 3.3V IO power from an external voltage regulator and uses the internal regulator to convert 3.3V to 1.2V for digital core and PLL power.

2.2.2 power on reset

The power on reset can be controlled from external reset pin, which is an asynchronous, active low system reset from the external host.

There is a software reset register in the OV430, which can also be controlled by an external host through the SCCB interface.

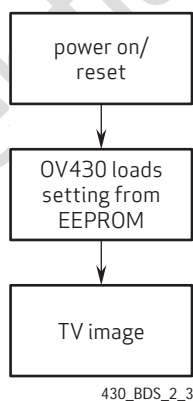
2.2.3 power-on reset sequence

In host mode, the OV430 should be connected with the image sensor as an image input, and to the TV as an image output. An EEPROM is required for storing settings for both the OV430 and sensor. Upon power on, the OV430 automatically searches for the EEPROM. Once found, it loads the settings into the sensor and itself respectively. No other power-on sequence is needed.

In host mode, reset is achieved through the hardware reset switch.

The host mode power-on/reset sequence is shown as **figure 2-3**.

figure 2-3 host mode power-on reset sequence



In slave mode, the external host controller is responsible for setting both the OV430 and the image sensor through SCCB bus. After power on, the data path of the OV430 defaults to reset status while the control path accepts settings. After configuration is done, the host can set 'low' on the data path reset to enable the OV430 device. The data path reset control bit is located in register 0x530F[7].

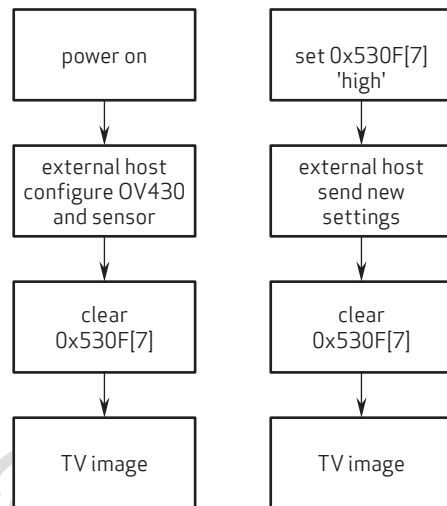
In slave mode, reset can be achieved through either the hardware reset switch or through software reset.

If using hardware reset, the external host is responsible for feeding all the settings to the OV430 and the image sensor before the device can function again.

If using software reset, the external host can set 'high' on the data path reset and feed in a new set of settings to the OV430 or image sensor. After the new settings are complete, the device can be released from reset by setting the data path reset back to 'low'.

The slave mode power-on/software reset sequence is shown in **figure 2-4**.

figure 2-4 slave mode power-on software reset sequence



430_BDS_2_4



note

using the software reset will not restore all settings to their default value.

2.2.4 operation modes of OV430 system

2.2.4.1 host mode

In host mode, the OV430 should be connected with the image sensor as an image input, and to the TV as image output. In addition, an EEPROM is required for storing settings for both the OV430 and the image sensor. Upon power on, the OV430 automatically searches for the EEPROM. Once found, it loads the settings into the sensor and itself respectively.

figure 2-5 host mode connections

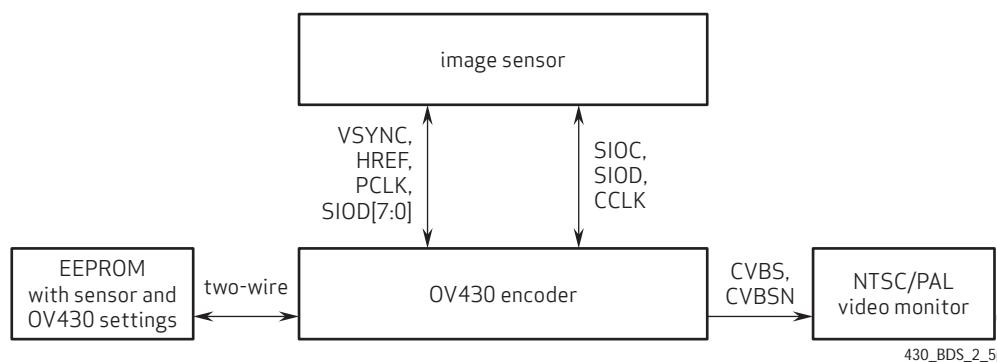


table 2-1 pin settings for host mode

pin	value	notes
TMODE	low	
HMODE	high	

2.2.4.2 slave mode

in slave mode, the external host controller is responsible for setting both the OV430 and the image sensor through the SCCB bus. An EEPROM is optional for storing OSD patterns.

figure 2-6 slave mode connections

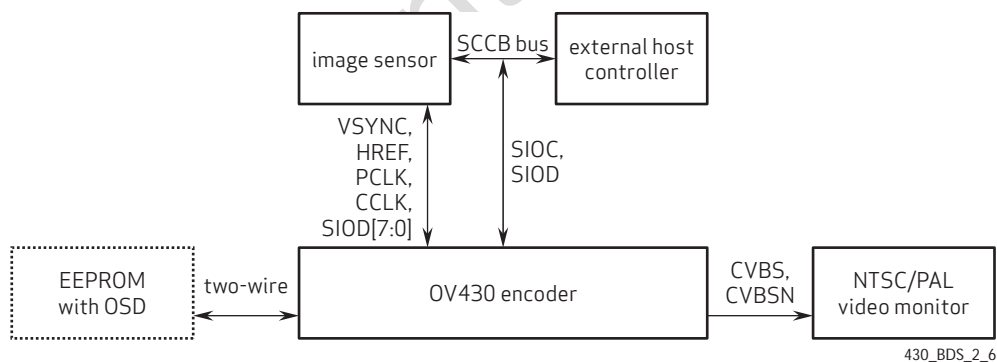


table 2-2 pin settings for slave mode

pin	value	notes
TMODE	low	
HMODE	low	

2.2.5 frame rate change mechanism in OV430 systems

In host/slave mode, OV430 should be connected to a digital sensor as image source. Different frame rates from sensor are supported. There are two ways for controlling the frame rates:

1. changing the sensor clock

The sensor image clock can be changed for outputting different frame rates. The register address is 0x11, its relationship with frame rate is as follows: $frame_rate = 60 / (\{0x11\} + 1)$. For example, set 0x11 to '01' for 30fps, '00' for 60fps.

2. inserting vertical dummy lines in original sensor image

Another method would be to insert vertical lines in sensor image. Settings registers are located at {0x2C, 0x2B}. Relationship is as follows: $frame_rate = (60 * default_value) / \{0x2C, 0x2B\}$. The default value for NTSC mode is 525; for PAL mode it is 540. Setting for 30fps would be {0x2C, 0x2B}=1050 for NTSC; {0x2C, 0x2B}=1080 for PAL.

2.2.6 system clock

There is one on-chip PLL in the OV430. It takes the reference clock input from the internal oscillator. The oscillator uses 24.5454 or 27MHz crystal as the input clock, depending upon the video mode selected.

2.3 format and frame rate

table 2-3 format and frame rate

mode	resolution	frame rate	TV resolution	pixel clock
NTSC	648x486	60 fps 30 fps 20 fps 15 fps 12 fps 10 fps	640 x 480	24.5454 MHz
NTSC D1	648x486	60 fps 30 fps 20 fps 15 fps 12 fps 10 fps	720 x 480	27 MHz
PAL D1	648x486	50 fps 25 fps 12.5 fps 10 fps	720 x 576	27 MHz

2.4 external interfaces

2.4.1 digital sensor interface

The OV430 supports input formats BT-656 (8-bit) and BT-601 (8-bit data with HREF, VSYNC). The only data type supported is YUV4:2:2.

2.4.2 SCCB interface

The SCCB interface is used to configure OV430 with an external host. The SCCB bus is also shared with the digital sensor.

2.4.3 two-wire interface

The OV430 supports a two-wire serial interface for OSD bitmap storage.

2.5 supported standards

The OV4300 supports NTSC 24.5454 MHz/ 27 MHz and PAL 27 MHz standard for TV image output. Settings for the different standards are shown in table [table 2-4](#).

table 2-4 supported standards table

pin	value	notes
VIDSEL	low for NTSC / high for PAL	
XSEL	low for 24.54 MHz / high for 27 MHz	

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3 image sensor output interface digital functions

3.1 video input timing

figure 3-1 video input timing diagram

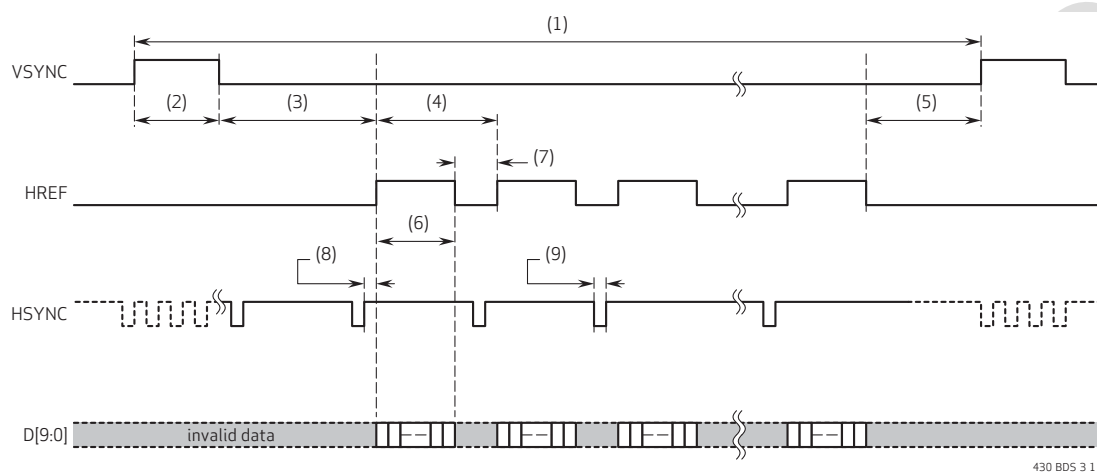


table 3-1 video input timing specifications

mode	timing
NTSC	(1) 450450 tp
	(2) 3432 tp
	(3) 28484 tp
	(4) 858 tp
	(5) 6912 tp
	(6) 640 tp
	(7) 218 tp
	(8) 106 tp
	(9) 48 tp
PAL	(1) 540000 tp
	(2) 4000 tp
	(3) 48170 tp
	(4) 1000 tp
	(5) 8190 tp
	(6) 640 tp
	(7) 360 tp
	(8) 106 tp
	(9) 48 tp



note

Timing values shown in **table 3-1** may vary depending upon register settings.

figure 3-2 data transfer on the SCCB

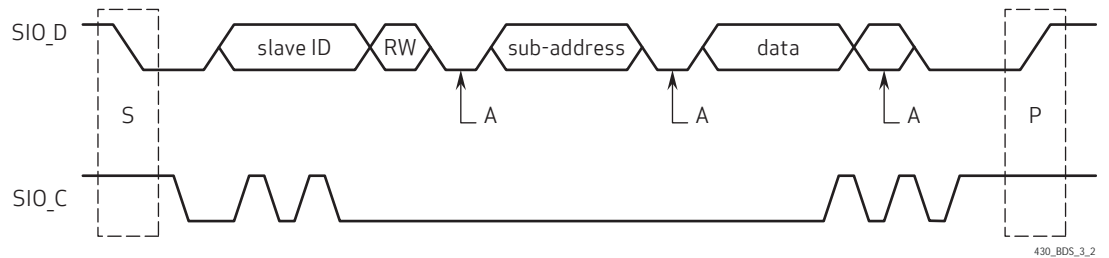
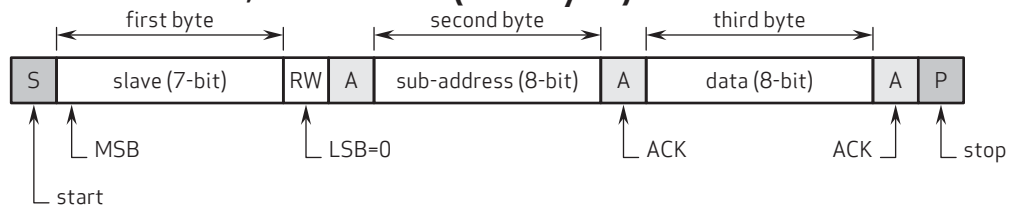
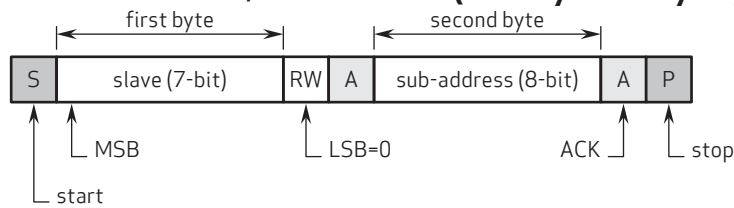


figure 3-3 SCCB protocol format

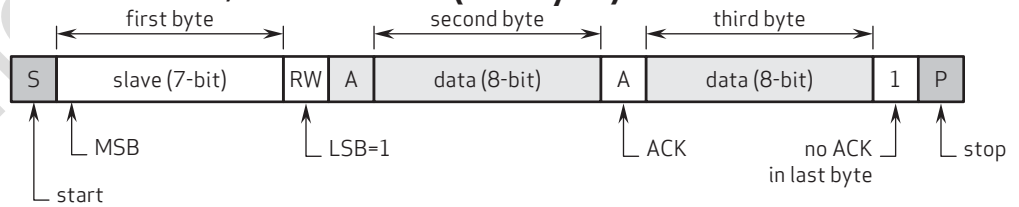
master transmit, slave receive (write cycle)



master transmit, slave receive (dummy write cycle)



master receive, slave transmit (read cycle)

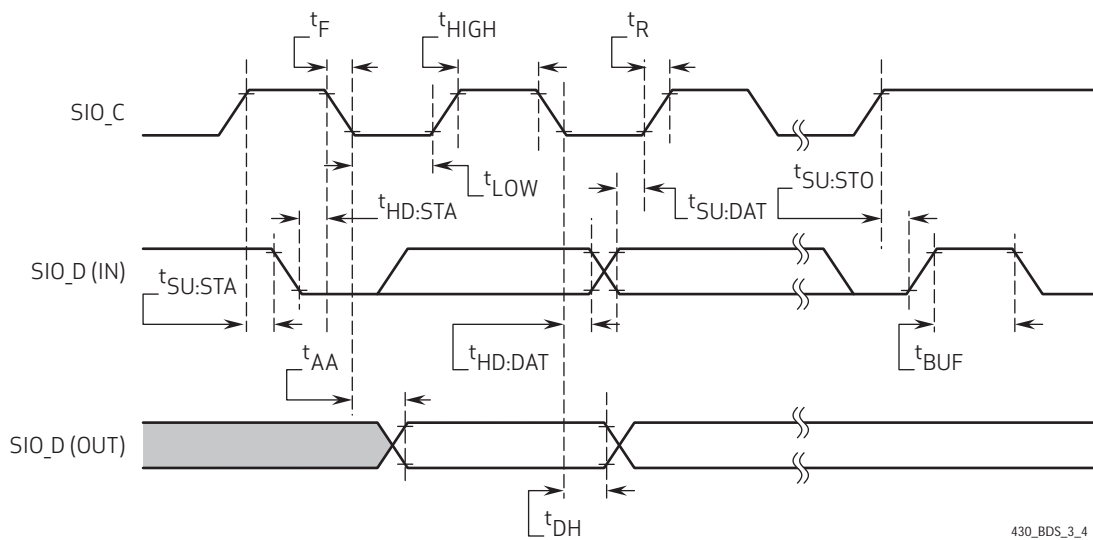


- slave ID 1000000X
- X RW bit, 1: read, 0: write
- S start condition
- A acknowledge bit
- P stop condition
- slave transmit
- master transmit
- master initiate

note: a register read usually consists of a dummy write cycle followed by a read cycle.

430_BDS_3_3

figure 3-4 SCCB timing diagram



430_BDS_3_4

table 3-2 SCCB interface timing specifications

symbol	parameter	min	typ	max	unit
f_{SIO_C}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			μ s
t_{HIGH}	clock high period	600			ns
t_{AA}	SIO_C low to data out valid	100		900	ns
t_{BUF}	bus free time before new START	1.3			μ s
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	data in hold time	0			μ s
$t_{SU:DAT}$	data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
t_R, t_F	SCCB rise/fall times			300	ns
t_{DH}	data out hold time	50			ns

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4 register tables

table 4-1 high byte decode

module name	function	address range
SCCB	SCCB master / SCCB slave	0x5100 ~ 0x51FF
SC	system controller	0x5300 ~ 0x53FF
LDMA	data from EEPROM loader	0x5400 ~ 0x54FF
OSD_overlay	OSD overlay	0x5600 ~ 0x56FF
TV_encoder	TV encoder	0x5700 ~ 0x57FF
OSD_SRAM	OSD SRAM	0x8000 ~ 0xC000

table 4-2 SCCB registers

address	register name	default value	R/W	description
0x5100	SCCB_CTRL	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Master support for 16-bit or 8-bit address slave Bit[1]: sccb_en_o Bit[0]: Slave address increase enable
0x5101	SCCB_SLAVE_ID	0x48	RW	SCCB Slave ID
0x5102	SCCB_MS_SPD	0x11	RW	SCCB Master Speed
0x5103	SCCB_MASTER_ID	0x42	RW	SCCB Master ID
0x5104	SCCB_LDMA_WTIMES	0x4D	RW	Numbers of SCCB Master Write Sensor Setting

table 4-3 SC registers

address	register name	default value	R/W	description
0x530E	SC_DVPTST	0x00	RW	SC DVP Test Control Register Bit[7]: Debug mode Bit[6]: Select sensor type to count the blanking time Bit[5]: Internal generate color bar enable Bit[4:0]: Debug mode

table 4-4 LDMA registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5400	LDMA_CTRL	0x01	RW	LDMA Control Bit[7:5]: Debug mode Bit[4]: Clear image first Bit[3]: Infinite loading image Bit[2]: FIFO debug mode Bit[1]: FIFO_clear Bit[0]: load_img_en
0x5401	SCCB ID	0x52	RW	Bit[7]: Restart selection Bit[6:0]: SCCB ID
0x5402	SCCB SPEED LOW BYTE	0x47	RW	Bit[7:0]: SCCB speed[7:0]
0x5403	SCCB MASTER CONTROL	0x01	RW	Bit[7]: Debug mode Bit[6]: NACK control Bit[5:2]: SCCB speed[11:8] Bit[1:0]: addr_byte
0x5405	SCCB RETRY	0x03	RW	Bit[7:2]: Debug mode Bit[1:0]: SCCB retry times in host mode
0x5407	IMAGE BASE ADDRESS BYTE 3	0x00	RW	Bit[7:0]: Image base address[31:24]
0x5408	IMAGE BASE ADDRESS BYTE 2	0x00	RW	Bit[7:0]: Image base address[23:16]
0x5409	IMAGE BASE ADDRESS BYTE 1	0x00	RW	Bit[7:0]: Image base address[15:8]
0x540A	IMAGE BASE ADDRESS BYTE 0	0x00	RW	Bit[7:0]: Image base address[7:0]
0x5411	ADDITIONAL BYTES FOR OFFSET AND IMAGE WIDTH	0x00	RW	Bit[7:3]: Debug mode Bit[2]: Additional image width byte number Bit[1:0]: Additional offset byte number
0x5412	BACKGROUND	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Image background value

table 4-4 LDMA registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5413	DELAY TIME BYTE 3	0x01	RW	Bit[7:0]: Delay time before normal images in host mode[31:24]
0x5414	DELAY TIME BYTE 2	0x9C	RW	Bit[7:0]: Delay time before normal images in host mode[23:16]
0x5415	DELAY TIME BYTE 1	0x66	RW	Bit[7:0]: Delay time before normal images in host mode[15:8]
0x5416	DELAY TIME BYTE 0	0x53	RW	Bit[7:0]: Delay time before normal images in host mode[7:0]
0x5417	DELAY CLEAR TIME BYTE 3	0x01	RW	Bit[7:0]: Delay time before clear images in host mode[31:24]
0x5418	DELAY CLEAR TIME BYTE 2	0x9C	RW	Bit[7:0]: Delay time before clear images in host mode[23:16]
0x5419	DELAY CLEAR TIME BYTE 1	0x66	RW	Bit[7:0]: Delay time before clear images in host mode[15:8]
0x541A	DELAY CLEAR TIME BYTE 0	0x53	RW	Bit[7:0]: Delay time before clear images in host mode[7:0]
0x5420	LOADING IMAGE AND SETTING STATUS	–	R	Bit[7:6]: Debug mode Bit[5:4]: Addr_byte_i in host mode Bit[3]: Load setting successful Bit[2]: Load setting busy Bit[1]: Loading one image busy Bit[0]: Loading image busy
0x5421	COMMAND FIFO DATA IN DEBUG MODE	–	R	Bit[7:0]: Command FIFO data in debug mode
0x5422	COMMAND FIFO STATUS	–	R	Bit[7:4]: Debug mode Bit[3:0]: Command FIFO status
0x5423	SCCB ID TRIED OUT	–	R	SCCB ID which has been tried out
0x5430	COMMAND SET START ADDRESS BYTE 3	0x00	RW	Bit[7:0]: Command set start address[31:24]
0x5431	COMMAND SET START ADDRESS BYTE 2	0x00	RW	Bit[7:0]: Command set start address[23:16]
0x5432	COMMAND SET START ADDRESS BYTE 1	0x00	RW	Bit[7:0]: Command set start address[15:8]
0x5433	COMMAND SET START ADDRESS BYTE 0	0x00	RW	Bit[7:0]: Command set start address[7:0]
0x5434	COMMAND CLEAR SET START ADDRESS BYTE 3	0x00	RW	Bit[7:0]: Command clear set start address[31:24]

table 4-4 LDMA registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5435	COMMAND CLEAR SET START ADDRESS BYTE 2	0x00	RW	Bit[7:0]: Command clear set start address[23:16]
0x5436	COMMAND CLEAR SET START ADDRESS BYTE 1	0x00	RW	Bit[7:0]: Command clear set start address[15:8]
0x5437	COMMAND CLEAR SET START ADDRESS BYTE 0	0x00	RW	Bit[7:0]: Command clear set start address[7:0]
0x5438	COMMAND SET LENGTH BYTE 3	0x00	RW	Bit[7:0]: Command set length[31:24]
0x5439	COMMAND SET LENGTH BYTE 2	0x00	RW	Bit[7:0]: Command set length[23:16]
0x543A	COMMAND SET START ADDRESS BYTE 1	0x00	RW	Bit[7:0]: Command set length[15:8]
0x543B	COMMAND SET LENGTH BYTE 0	0x00	RW	Bit[7:0]: Command set length[7:0]
0x543C	COMMAND CLEAR LENGTH BYTE 3	0x00	RW	Bit[7:0]: Command clear set length[31:24]
0x543D	COMMAND CLEAR LENGTH BYTE 2	0x00	RW	Bit[7:0]: Command clear set length[23:16]
0x543E	COMMAND CLEAR LENGTH BYTE 1	0x00	RW	Bit[7:0]: Command clear set length[15:8]
0x543F	COMMAND CLEAR LENGTH BYTE 0	0x00	RW	Bit[7:0]: Command clear set length[7:0]

table 4-5 OSD overlay registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5600	OSD_CTRL0	0x00	RW	Bit[7]: OSD_enable Bit[6]: vert_scale_en Bit[5]: mask_enable Bit[4]: normal_inverse Bit[3]: color_bar_en Bit[2]: color_bar_type Bit[1]: color_sel_reg Bit[0]: OSD_bypass_mode
0x5601	OSD_CTRL1	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: image_hsize[9:8]
0x5602	OSD_CTRL2	0x80	RW	Bit[7:0]: image_hsize[7:0]

table 4-5 OSD overlay registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5603	OSD_CTRL3	0x01	RW	Bit[7:1]: Debug mode Bit[0]: image_vsize[8]
0x5604	OSD_CTRL4	0xE0	RW	Bit[7:0]: image_vsize[7:0]
0x5605	OSD_CTRL5	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: mask_hstart[9:8]
0x5606	OSD_CTRL6	0x00	RW	Bit[7:0]: mask_hstart[7:0]
0x5607	OSD_CTRL7	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: mask_hsize[9:8]
0x5608	OSD_CTRL8	0xF0	RW	Bit[7:0]: mask_hsize[7:0]
0x5609	OSD_CTRL9	0x00	RW	Bit[7:1]: Debug mode Bit[0]: mask_vstart[8]
0x560A	OSD_CTRLA	0x00	RW	Bit[7:0]: mask_vstart[7:0]
0x560B	OSD_CTRLB	0x00	RW	Bit[7:1]: Debug mode Bit[0]: mask_vsize[8]
0x560C	OSD_CTRLC	0xF0	RW	Bit[7:0]: mask_vsize[7:0]
0x560D	OSD_CTRLD	0x00	RW	Bit[7:0]: OSD_FB_offset[15:8]
0x560E	OSD_CTRL E	0x00	RW	Bit[7:0]: OSD_FB_offset[7:0]
0x5610	OSD_CTRL10	0x80	RW	Bit[7:0]: look_up_table0[7:0] V
0x5611	OSD_CTRL11	0x80	RW	Bit[7:0]: look_up_table0[15:8] U
0x5612	OSD_CTRL12	0x00	RW	Bit[7:0]: look_up_table0[23:16] Y
0x5613	OSD_CTRL13	0x6A	RW	Bit[7:0]: look_up_table1[7:0] V
0x5614	OSD_CTRL14	0xFC	RW	Bit[7:0]: look_up_table1[15:8] U
0x5615	OSD_CTRL15	0x1D	RW	Bit[7:0]: look_up_table1[23:16] Y
0x5616	OSD_CTRL16	0x14	RW	Bit[7:0]: look_up_table2[7:0] V
0x5617	OSD_CTRL17	0x2A	RW	Bit[7:0]: look_up_table2[15:8] U
0x5618	OSD_CTRL18	0x95	RW	Bit[7:0]: look_up_table2[23:16] Y
0x5619	OSD_CTRL19	0xFF	RW	Bit[7:0]: look_up_table3[7:0] V
0x561A	OSD_CTRL1A	0x54	RW	Bit[7:0]: look_up_table3[15:8] U
0x561B	OSD_CTRL1B	0x4C	RW	Bit[7:0]: look_up_table3[23:16] Y
0x561C	OSD_CTRL1C	0x00	RW	Bit[7:0]: look_up_table4[7:0] V
0x561D	OSD_CTRL1D	0xAA	RW	Bit[7:0]: look_up_table4[15:8] U
0x561E	OSD_CTRL1E	0xB2	RW	Bit[7:0]: look_up_table4[23:16] Y

table 4-5 OSD overlay registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x561F	OSD_CTRL1F	0xEA	RW	Bit[7:0]: look_up_table5[7:0] V
0x5620	OSD_CTRL20	0xD4	RW	Bit[7:0]: look_up_table5[15:8] U
0x5621	OSD_CTRL21	0x69	RW	Bit[7:0]: look_up_table5[23:16] Y
0x5622	OSD_CTRL22	0x94	RW	Bit[7:0]: look_up_table6[7:0] V
0x5623	OSD_CTRL23	0x00	RW	Bit[7:0]: look_up_table6[15:8] U
0x5624	OSD_CTRL24	0xE1	RW	Bit[7:0]: look_up_table6[23:16] Y
0x5625	OSD_CTRL25	0x80	RW	Bit[7:0]: look_up_table7[7:0] V
0x5626	OSD_CTRL26	0x80	RW	Bit[7:0]: look_up_table7[15:8] U
0x5627	OSD_CTRL27	0xFF	RW	Bit[7:0]: look_up_table7[23:16] Y
0x5628	OSD_CTRL28	0x80	RW	Bit[7:4]: op_code_lut1 Bit[3:0]: op_code_lut0
0x562A	OSD_CTRL2A	0x00	RW	Bit[7:0]: OSD_blinking_on[7:0]
0x562B	OSD_CTRL2B	0x00	RW	Bit[7:0]: OSD_blinking_total[7:0]
0x562C	OSD_CTRL2C	0x00	RW	Bit[7:0]: osd_h_offset[7:0]
0x562D	OSD_CTRL2D	0x00	RW	Bit[7:0]: osd_v_offset[7:0]

table 4-6 TV encoder registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5700	R0	0xC8	RW	White Level
0x5701	R1	0x46	RW	Normal Level, Black Level
0x5702	R2	0x3C	RW	Blank Level
0x5703	R3	0x04	RW	Sync Level
0x5704	R4	0x23	RW	Burst Level
0x5705	R5	0xFF	RW	Max Level
0x5706	R6	0x7F	RW	Chroma Saturation
0x570B	RB	0x00	RW	Phase Adjust Changing these registers is not recommended
0x5711	R11	0x52	RW	Bit[7:0]: Y coefficient[9:2]
0x5712	R12	0x54	RW	Bit[7:0]: U coefficient[9:2]

table 4-6 TV encoder registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5713	R13	0x54	RW	Bit[7:0]: V coefficient[9:2]
0x5714	R14	0x02	RW	Bit[7:6]: Debug mode Bit[5:4]: V coefficient[1:0] Bit[3:2]: U coefficient[1:0] Bit[1:0]: Y coefficient[1:0]
0x5715	R15	0x13	RW	Bit[7:6]: Debug mode Bit[5:0]: VBLK length
0x5716	R16	0x00	RW	Bit[7]: Debug mode Bit[6:4]: Color bar option Bit[3:1]: Debug mode Bit[0]: Color bar enable
0x5718	R18	0x74	RW	HSYNC Control
0x5719	R19	0x40	RW	Burst Length
0x571A	R1A	0x28	RW	Fporch Length
0x571B	R1B	0x0E	RW	Bporch Length

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5 operating specifications

5.1 absolute maximum ratings

table 5-1 absolute maximum ratings

parameter		absolute maximum rating ^a
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V _{DD-A}	4.5V
	V _{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V _{DD-IO} +1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		264.5°C

- a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 functional temperature

table 5-2 functional temperature

parameter	range
operating temperature range	-30°C to +70°C

5.3 DC characteristics

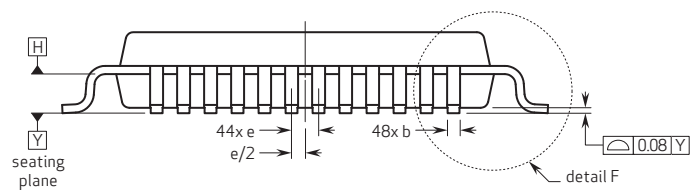
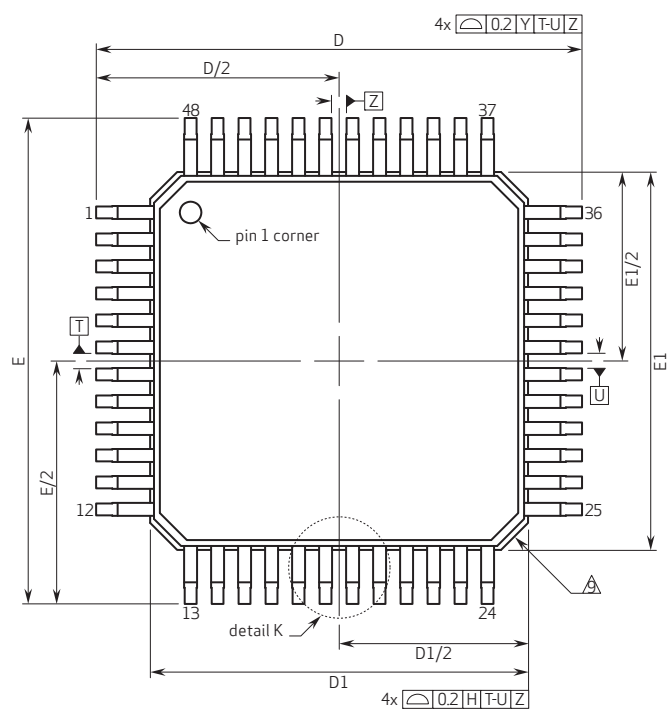
table 5-3 DC characteristics

symbol	parameter	condition	min	typ	max	unit
supply						
AVDD	supply voltage (analog)	3.3V ±10%	3.0	3.3	3.6	V
PADVDD	supply voltage (digital I/O)	3.3V ±10%	3.0	3.3	3.6	V
CVDD and PLLVDD	supply voltage (digital core)	1.2V ±10%	1.08	1.2	1.32	V
I _{CVDD}	active (operating) current			TBD		mA
digital inputs (typical conditions: AVDD = 3.3V, PADVDD =3.3V)						
V _{IH}	input voltage HIGH	CMOS	0.7 x PADVDD_IO			V
V _{IL}	input voltage LOW	CMOS			0.3 x PADVDD_IO	V
digital outputs (standard loading 25 pF)						
V _{OH}	output voltage HIGH	CMOS		TBD		V
V _{OL}	output voltage LOW	CMOS		TBD		V

6 mechanical specifications

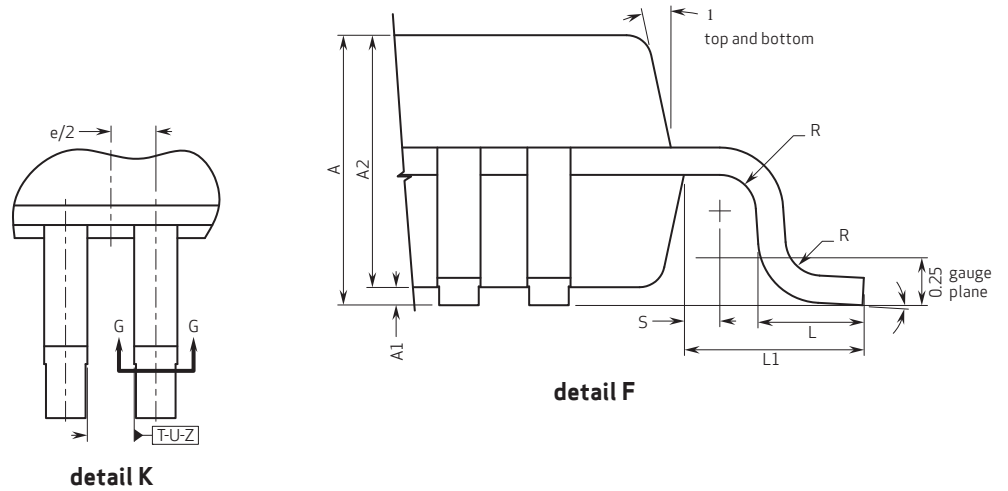
6.1 physical specifications

figure 6-1 package specifications view 1

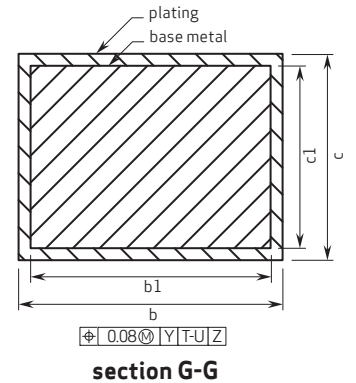


430_DS_3_1

figure 6-2 package specifications view 2



- note 1** all dimensions are in millimeters.
- note 2** interpret dimensions and tolerances per ASME Y 14.5 M - 1994.
- note 3** datum plane H is located at the bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
- note 4** datum T, U and Z to be determined at datum place H.
- note 5** dimensions D and E to be determined at seating plane Y.
- note 6** dimensions D1 and E1 do not include mold protrusion, allowable protrusion is 0.25 per side. dimensions D1 and E1 do include mold mismatch and are determined at datum plane H.
- note 7** dimension b does not include dam bar protrusion. dam bar protrusion shall not cause the b dimension to exceed 0.35.
- note 8** minimum solder plate thickness is 0.0076.



430_DS_3.2

table 6-1 package dimensions (sheet 1 of 2)

parameter	min	max
A	1.4	1.6
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.2
c1	0.09	0.16
D	9 BSC	

table 6-1 package dimensions (sheet 2 of 2)

parameter	min	max
D1		7 BSC
e		0.5 BSC
E		9 BSC
E1		7 BSC
L	0.5	0.7
L1		1 REF
R	0.15	0.25
S		0.2 REF
0	1	5
01		12 REF

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figure 6-3 IR reflow ramp rate requirements

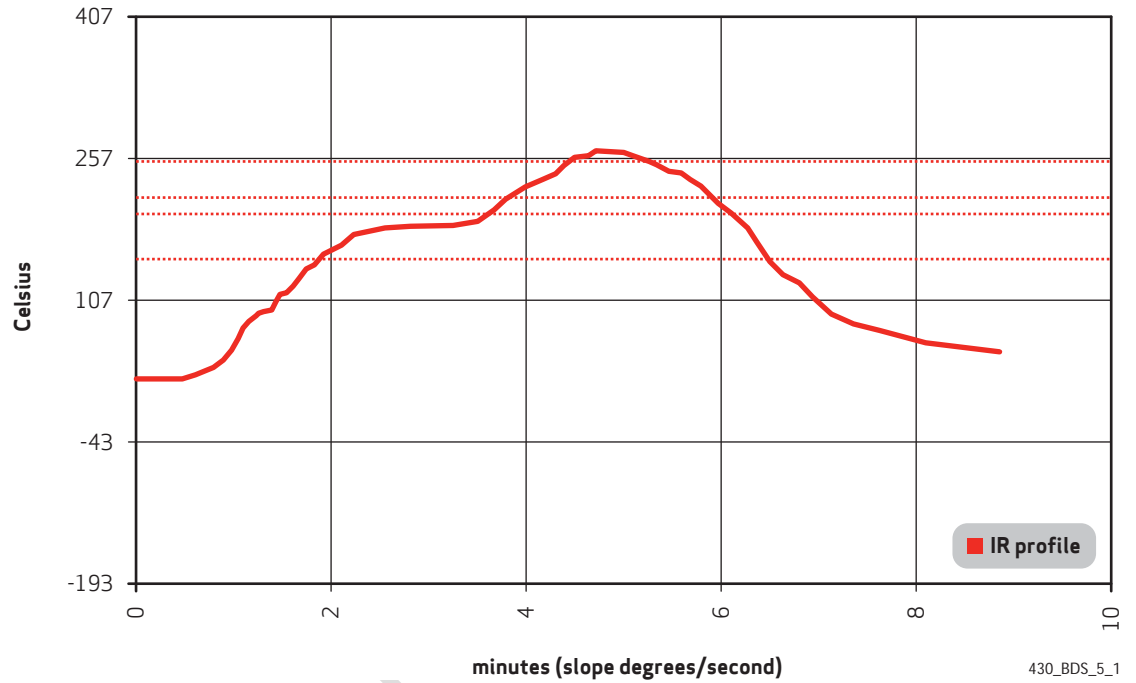


table 6-2 IR reflow ramp rate requirements

thermo tracker number	peak	max rising slope	max slope	rising time between 150°/200°	total time above 217°	total time above 255°
1	-11.4	0.00	0.00	0.00	0.00	0.00
2	-5.3	0.00	0.00	0.00	0.00	0.00
3	264.5	2.78	2.78	105.63	124.40	51.07

revision history

version 1.0 05.10.2010

- initial release

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